Large Current External FET Controller Type Switching Regulators

High-frequency Step-down Switching Regulator(Controller type)

BD9850FVM

Dual-output Step-up, Negative, Step-down Switching Regulator(Controller type)

BD9851EFV

●Description

The BD9850FVM is a 1-channel DC/DC step-down switching regulator controller, while the BD9851EFV is a 2-channel DC/DC step-down switching regulator controller. The BD9850FVM is adaptable for a maximum switching frequency of 2 MHz and the BD9851EFV for that of 3 MHz. Both provide space saving in all applications.

●Features

1) Adaptable for 2-MHz switching frequency (externally variable) (BD9850FVM)
   Adaptable for 3-MHz switching frequency (externally variable) (BD9851EFV)
2) FET direct drive
3) High-accuracy reference voltage (Accuracy: ±1%)
4) Built-in Under Voltage Lock Out circuit (UVLO)
5) Built-in Thermal Shutdown circuit (TSD)
6) The BD9851EFV provides two channels:
   Channel 1 available for selection of step-down/step-up switching
   Channel 2 available for selection of step-down/inverting switching.
7) Compact MSOP8 package (BD9850FVM) / HTSSOP-B20 package (BD9851EFV)

●Applications

TFT panel, TA / Router, digital consumer electronics, PC, and portable CD/ DVD/ DVC

●Product lineup

	BD9850FVM	BD9851EFV
Input range	4V to 9V	4V to 18V
Oscillation frequency range	100kHz to 2MHz	10kHz to 3MHz
External synchronization	Not provided	Not provided
Standby function	Not provided	Provided
Operating temperature	−40℃ to 85℃	−40℃ to 85℃
Package	MSOP8	HTSSOP-B20

● Absolute maximum ratings (Ta=25˚C)

◯ BD9850FVM

Item	Symbol	Rating	Unit
Power supply voltage	Vcc	10	V
Storage temperature	Tstg	−55 to +150	ºC
Operating temperature	Topr	−40 to +85	ºC
Power dissipation	Pd	587 *	mW
Maximum junction temperature	Tjmax	+150	ºC

*Reduce by 4.7 mW/ºC over 25ºC (When mounted on PCB of 70mm×70mm×1.6mm)

◯ BD9851EFV

Item	Symbol	Rating	Unit
Power supply voltage (Between Vcc and GND)	Vcc	20	V
Between VREF and GND	VREF	7	V
Between OUT1 and PVcc1 Between OUT2 and PVcc2	Vouth	20	V
Between OUT1, OUT2 and PGND	Voutl	20	V
Power dissipation	Pd	1000 (*)	mW
Operating temperature	Topr	−40 to +85	ºC
Maximum junction temperature	Tjmax	+150	ºC
Storage temperature	Tstg	−55 to +150	ºC

(*)Reduce by 8.0 mW/ºC over 25ºC (When mounted on PCB of 70mm×70mm×1.6mm)

● Recommended operating range

◯ BD9850FVM

Item	Symbol	Limits			Unit
		min.	Typ.	max.	
Power supply voltage	Vcc	4	7	9	V
Oscillation frequency	fosc	100	–	2000	kHz
Operating temperature	Topr	−40	–	+85	ºC

◯ BD9851EFV

Item	Symbol	Limits			Unit
		min.	Typ.	max.	
Power supply voltage	Vcc	4	12	18	V
Oscillation frequency	fosc	10	300	3000	kHz
Timing resistor	RRT	3.3	–	47	kΩ
Timing capacitor	CCT	33	–	10000	pF

◎ BD9850FVM

Electrical characteristics (Unless otherwise specified, Ta=25℃, Vcc=7V, fosc=600kHz)

Item	Symbol	Limits			Unit	Conditions
		min.	Typ.	max.		
[Oscillator block]						
Oscillation frequency	fosc	510	600	690	kHz	R_{RT} = 24kΩ
Frequency regulation	FDV	–5	0	5	%	Vcc = 4V to 9V
Oscillator amplitude voltage	Vpptr	–	0.5	–	V	*
[Soft start / SW block]						
CTL / SS pin sink current	ISS	–1.90	–1.00	1.00	μA	$V_{CTL/SS}$ = 1.5V
CTL / SS pin clamp voltage	VSS	2.2	2.4	2.6	V	
CTL threshold voltage	VCTLTH	1.2	1.3	1.4	V	
[PWM comparator block]						
0% threshold voltage	D0	1.5	1.6	1.7	V	fosc = 600kHz
100% threshold voltage	D100	2.0	2.1	2.2	V	fosc = 600kHz
[Error Amp block]						
Threshold voltage	V_{IN}	0.98	1.00	1.02	V	AV = 0dB *
Frequency bandwidth	BW	1.5	3.0	–	MHz	*
Voltage gain	Av	–	70	–	dB	
Input bias current	IIB	–150	–70	–	hA	
Maximum output voltage	VCH	2.3	2.4	2.6	V	
Minimum output voltage	VCL	–	0.03	0.20	V	
Output source current	IOI	–3.1	–1.6	–1.0	mA	V_{FB} = 1.0V
Output sink current	IOO	12	50	125	mA	V_{FB} = 1.0V
[V_{REF} block]						
V_{REF} output voltage	V_{REF}	2.475	2.500	2.525	V	I_{VREF} = 0mA
F_{REF} load regulation	ΔV_{REFI0}	–	–	10	mV	I_{VREF} = 0mA to –1mA
V_{REF} current capacitance	I_{VREF}	–45	–16	–1	mA	
[Total device]						
Standby current	ICCS	420	610	960	μA	
Average supply current	ICCA	3.4	5.0	7.8	mA	At no load
[Output block]						
ON resistance	R_{ON}	0.9	2.5	8.0	Ω	
Output transient time	Tr/Tf	–	20	–	nsec	Cout = 1000pF *
[Under voltage lockout block]						
Threshold voltage	VUT	3.7	3.8	3.9	V	Vcc sweep down
Hysteresis width	VUThy	0.05	0.10	0.15	V	

*Design guarantee
*Not designed to be radiation-resistant.

◎ BD9851EFV

Electrical characteristics (Unless otherwise specified, Ta=25℃, Vcc=12V, fosc=300kHz, STB=3V)

Item	Symbol	Limits			Unit	Conditions
		min.	Typ.	max.		
[Total device]						
Standby mode circuit current	Iccst	–	–	5	μA	STB=0V
Operation mode circuit current	Icc	1.5	2.5	4.1	mA	FB1, FB2=0V
[Reference voltage block]						
Output voltage	V_{REF}	2.475	2.500	2.525	V	Io=−0.1mA
Input stability	DVli	–	–	10	mV	Vcc=4Vto18V, Io=−0.1mA
Load stability	DVlo	–	–	10	mV	Io=−0.1mA to −1mA
Short circuit mode output current	Ios	−45	−12	−3	mA	
[Oscillator block]						
Oscillation frequency	fosc	270	300	330	kHz	R_{RT}=24kΩ, C_{CT}=220pF
Oscillation frequency regulation	Dfosc	−2	0	2	%	Vcc=4Vto18V
[Error Amp block]						
Threshold voltage	Vthea	0.98	1.00	1.02	V	Ch1
Input offset voltage	Vofst	−10	0	10	mV	Ch2
Common-mode input voltage range	Vcm	0.3	–	2.0	V	Ch2
Input bias current	Ibias	−150	−70	–	nA	
Voltage gain	Av	60	75	90	dB	DC *Design guarantee
Frequency bandwidth	Bw	3	6	13	MHz	MHz *Design guarantee
Maximum output voltage	Vfbh	V_{REF}−0.1	–	V_{REF}	V	
Minimum output voltage	Vfbl	–	–	0.1	V	
Output sink current	Isink	1.6	6	16	mA	FB pin
Output source current	Isource	−260	−160	−90	μA	FB pin
[PWM comparator block]						
0% threshold voltage	Vth0	1.21	1.31	1.41	V	FB voltage
100% threshold voltage	Vth100	1.74	1.84	1.94	V	FB voltage
DTC bias current	Idtc	−1	–	1	μA	
[FET driver block]						
ON resistance	R_{ON}N	1.5	3	3	Ω	When OUT=Lo
	R_{ON}P	1	2	2	Ω	When OUT=Hi
SEL1 input voltage range	Vselh	Vcc−0.2	–	–	V	In step-down switching
	Vsell	0	–	–	V	In step-down switching
[Control block]						
Threshold voltage	Vstb	0.6	1.5	1.5	V	
Sink current	Istb	6	15	15	μA	STB=3V
[Short circuit protection circuit (SCP) block]						
Timer start voltage	Vtime	2.2	2.3	2.3	V	FB voltage
Threshold voltage	Vthscp	1.4	1.5	1.5	V	SCP voltage
Standby mode voltage	Vstscp	–	10	10	mV	SCP voltage
Source current	Vsoscp	−3.2	−2.0	−2.0	μA	SCP=0.75V
[Under voltage lockout block (UVLO)]						
Threshold voltage	Vuvlo	3.58	3.7	3.7	V	Vcc sweep down
Hysteresis width	DVuvlo	0.05	0.11	0.11	V	

*Design guarantee

● Characteristic data

(BD9850FVM)

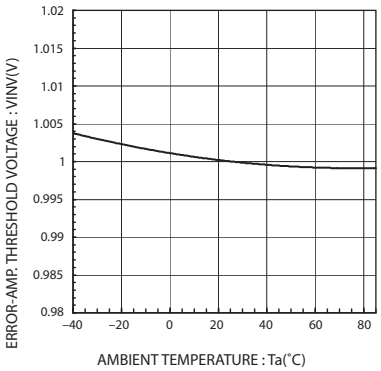


Fig.1 Error Amp threshold voltage vs. Ambient temperature

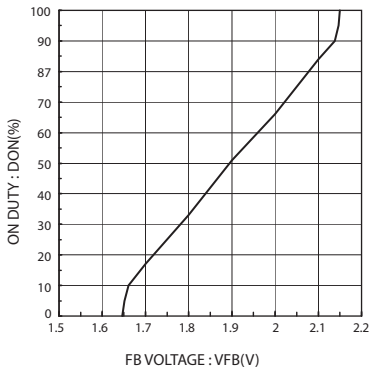


Fig.2 FB voltage vs. ON Duty

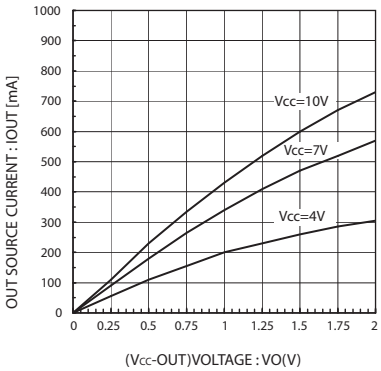


Fig.3 (Vcc-OUT) Voltage vs. Output source current

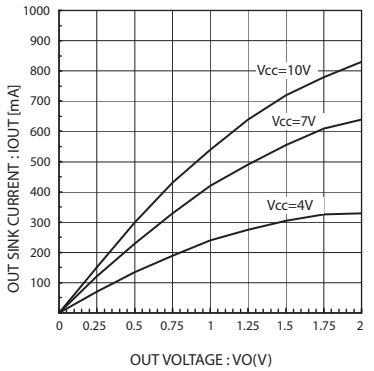


Fig.4 Output voltage vs. Output sink current

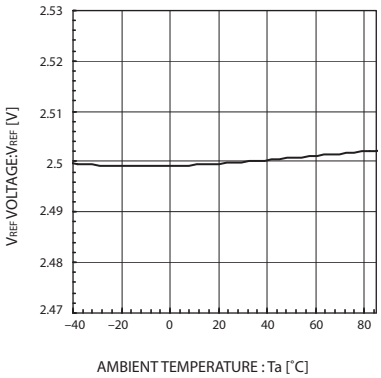


Fig.5 VREF vs. Ambient temperature

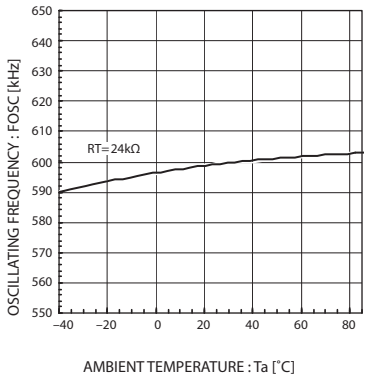


Fig.6 Oscillation frequency vs. Ambient temperature

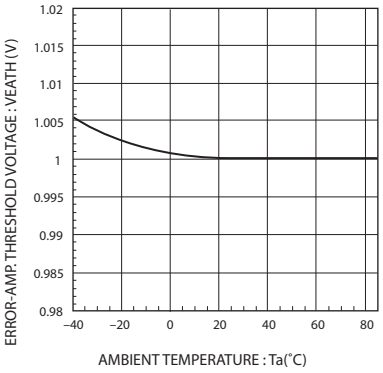


Fig.7 Error Amp threshold voltage vs. Ambient temperature

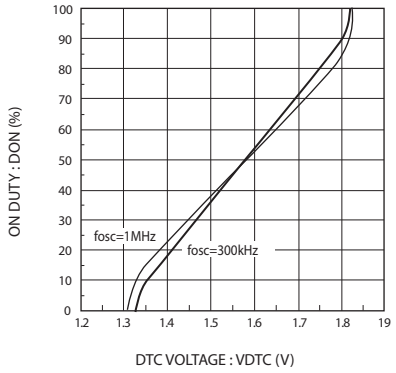


Fig.8 FB voltage vs. ON Duty

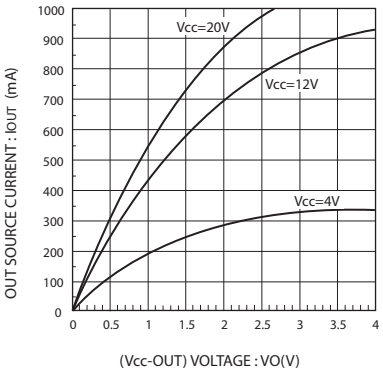


Fig.9 (Vcc-OUT) Voltage vs. Output source current

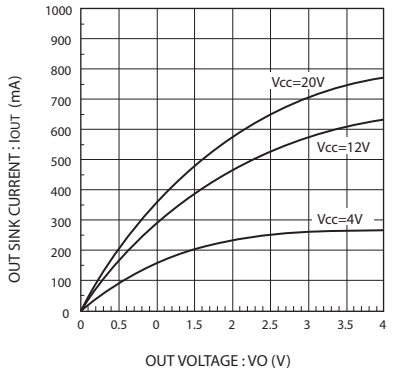


Fig.10 Output voltage vs. Output sink current

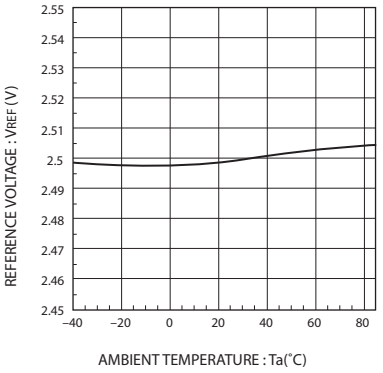


Fig.11 VREF vs. Ambient temperature

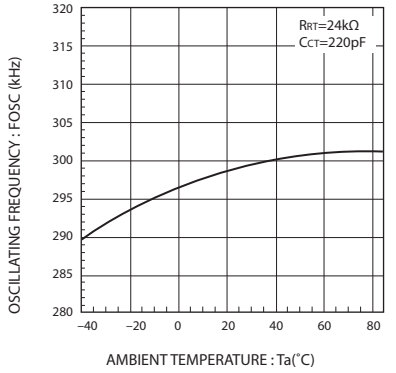


Fig.12 Oscillation frequency vs. Ambient temperature

●Block diagram / Pin assignment

(BD9850FVM)

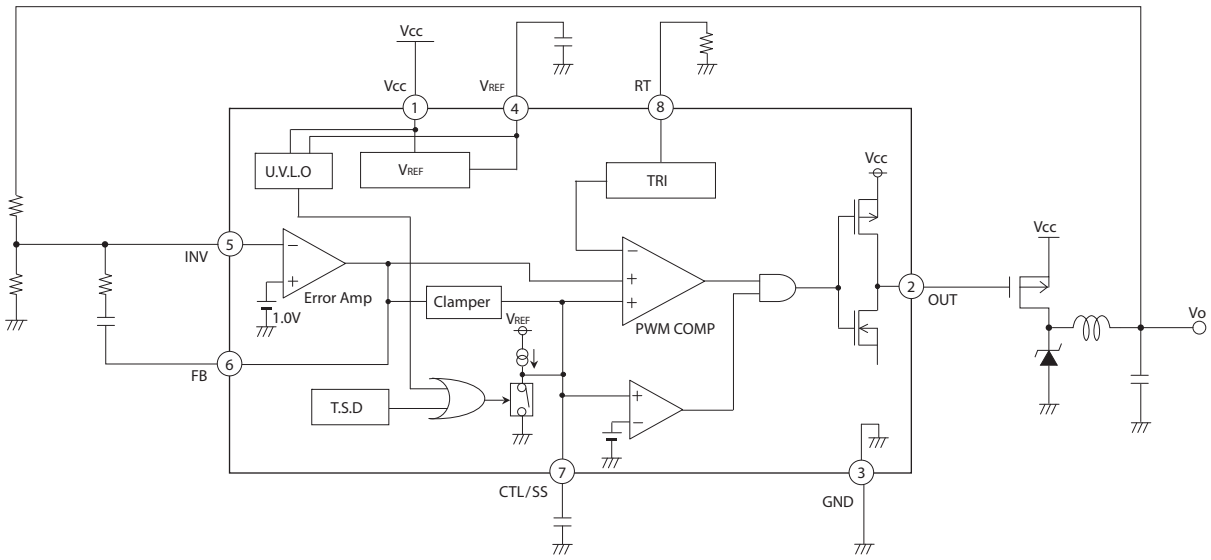
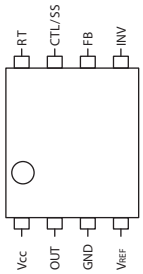


Fig.13 BD9850FVM Block diagram



Pin No.	Pin name	Function
1	Vcc	Power supply
2	OUT	FET driver drive output
3	GND	Ground
4	V_{REF}	Reference voltage (2.5V±1%) output
5	INV	Error Amp inverting input
6	FB	Error Amp output
7	CTL/SS	Control/Soft start common
8	RT	Oscillation frequency setting resistor connection

(BD9851EFV)

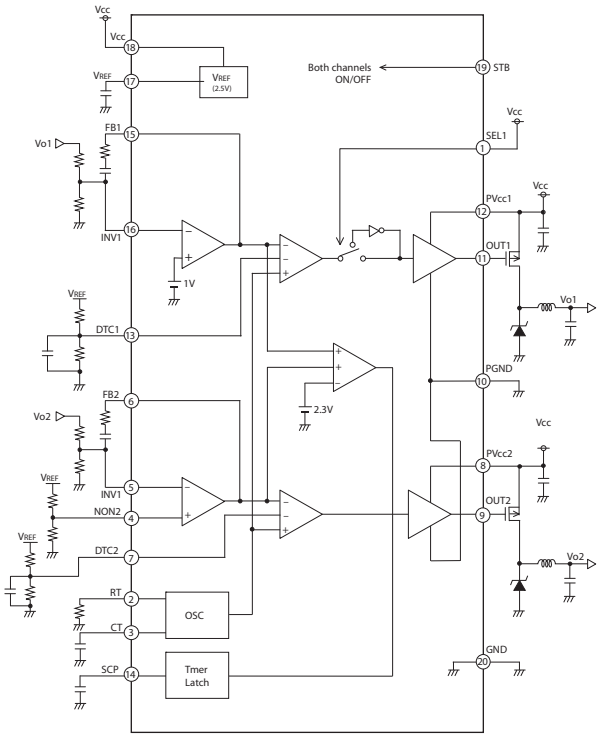
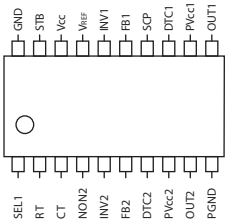


Fig.14 BD9851EFV Block diagram



Pin No.	Pin name	Function
1	SEL1	CH1 drive FET setting (Vcc short: P-ch drive, GND short: N-ch drive)
2	RT	Oscillation frequency setting resistor connection
3	CT	Oscillation frequency setting capacitor connection
4	NON2	Error Amp non-inverting input (CH2)
5	INV2	Error Amp inverting input (CH2)
6	FB2	Error Amp output (CH2)
7	DTC2	Maximum duty/soft start setting (CH2)
8	$PV_{CC}2$	FET driver block power supply input (CH2)
9	OUT2	FET driver block output (CH2)
10	PGND	FET driver block ground
11	OUT1	FET driver block output (CH1)
12	$PV_{CC}1$	FET driver block power supply input (CH1)
13	DTC1	Maximum duty/soft start setting (CH1)
14	SCP	Short circuit protection timer setting capacitor connection
15	FB1	Error Amp output (CH1)
16	INV1	Error Amp inverting input (CH1)
17	VR_{EF}	Reference voltage (2.5V±1%) output
18	V_{CC}	Power supply input
19	STB	ON/OFF control
20	GND	Ground
–	FIN on reverse	Make FIN on the reverse open or ground to GND (pin 20) (However, open FIN on the reverse will degrade radiation performance.)

● Description of operations

1) Reference voltage block
The reference voltage block generates a constant voltage with temperature compensated through inputting the power supplied from the Vcc pin. The output voltage is 2.5 V, with a ±1% accuracy. To cancel noises, insert a capacitor with a low ESR (several tens of mΩ) between the VREF and GND pins. It is recommended to use a ceramic capacitor of 1μF for this purpose.

2) Triangular wave oscillator block
By connecting the resistor and capacitor of frequency settings to the RT and CT pins (only to RT pin on the BD9850FVM), a triangular wave will be generated and then input to the PWM comparators of Channels 1 and 2.

3) Error Amp block
The Error Amp block detects the output voltage of the INV pin, amplifies an error with the set output voltage, and then outputs the error from the FB pin. The comparison voltage is 1 V, with a ±2% accuracy. (The Channel 2 of the BD9851EFV uses the NON pin input voltage as a reference.)
Inserting a resistor and capacitor between the INV and FB pins will conduct phase compensation.

4) PWM comparator block
The PWM comparator block converts the output voltage (FB voltage) into a PWM waveform and outputs it to the FET driver.
<Dead time control> (Only available on the BD9851EFV)
Inputting a voltage, divided by resistance of the VREF pin in the DTC pin, will allow maximum ON duty setting.
<Soft start (BD9850FVM)>
Inserting a capacitor between the CTL/SS and GND pins will allow the soft start function to control the rising output voltage.
<Soft start (BD9851EFV)>
Inserting a capacitor between the DTC and GND pins will allow the soft start function to control the rising output voltage. Furthermore, the overshoot of output voltage at startup can be derated. Adding a Schottky diode between the FB and DTC pins will make it possible to suppress the overshoot rate (only available with step-down application).

5) FET driver block
This block is a push-pull type driver enabling direct drive of external MOS FET.
<Setting of step-down/step-up switching (Only available for Channel 1 of BD9851EFV)>
For the Channel 1, SEL1 pin setting will determine the application function.
Set the SEL1 pin to step-down (P-ch drive) mode for short-circuiting Vcc or to step-up (N-ch drive) mode for short-circuiting GND.
Furthermore, be sure to short-circuit the SEL1 pin to Vcc or GND pin.

6) Standby function
(BD9850FVM)
The CTL/SS pin allows for output ON/OFF control. Set the CTL/SS pin voltage to "H" to activate the output ON control.
(BD9851EFV)
The STB pin allows for output ON/OFF control. Set the STB pin voltage to "H" to activate the output ON control.
The standby mode circuit current should be set to less than 5 μA.

7) Short circuit protection circuit (SCP) (Only available on BD9851EFV)
The SCP is a timer-latch type short circuit protection circuit.
If the output voltage of either channel drops below the set voltage, the Error Amp will be activated to increase the FB voltage and initiate charging the capacitor connected to the SCP pin with a 2 μA current. When the SCP pin voltage exceeds 1.5 V, the latch circuit will be activated to fix the output of both channels at OFF and, at the same time, the DTC pin at "L" level.
In order to rest the latch circuit, set the STB pin to "L" level once, and then to "H" level. Or, turn ON the power supply again.
Furthermore, if the short circuit protection circuit is not used, short-circuit the SCP pin to the GND pin.

8) Under Voltage Lock Out (UVLO) circuit
The UVLO is a protection circuit to prevent the IC from malfunctioning when the power supply turns ON or if an instantaneous power interruption occurs.
When the Vcc voltage falls below 3.8 V (or 3.7 V on the BD9851EFV), the output of both channels will be fixed at "OFF" and, at the same time, the DTC pin at "L" level. Hysteresis width of 0.1 V (or 0.11 V on the BD9851EFV) is provided for the detection voltage and release voltage of the UVLO in order to prevent malfunctions of the IC which may result from variations in the input voltage due to threshold online.
Furthermore, if the latch circuit is activated through the short circuit protection circuit, the circuit will be reset by this UVLO.

9) Thermal shutdown circuit (TSD)
The TSD is a protection circuit to prevent the destruction of the IC due to abnormal heat generation.
If the TSD detects an abnormal heat generation (175˚C) on the chip, the output of both channels will be fixed at "OFF" and, at the same time, the DTC pin at "L" level. Hysteresis width (15˚C) is provided for the superheat detection and release temperatures in order to prevent malfunctions of the IC which may result from variations in the input voltage due to threshold online.
Furthermore, if the latch circuit is activated through the short circuit protection circuit, the circuit will be reset by this TSD.

● Timing chart

• In startup/normal operation
(BD9850FVM)

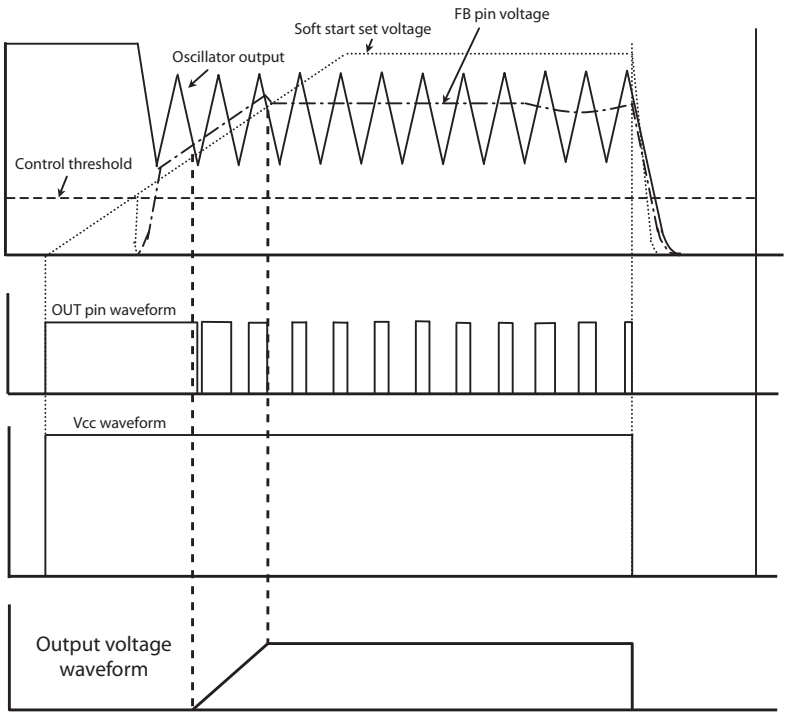


Fig.15 BD9850FVM Timing chart

(BD9851EFV)

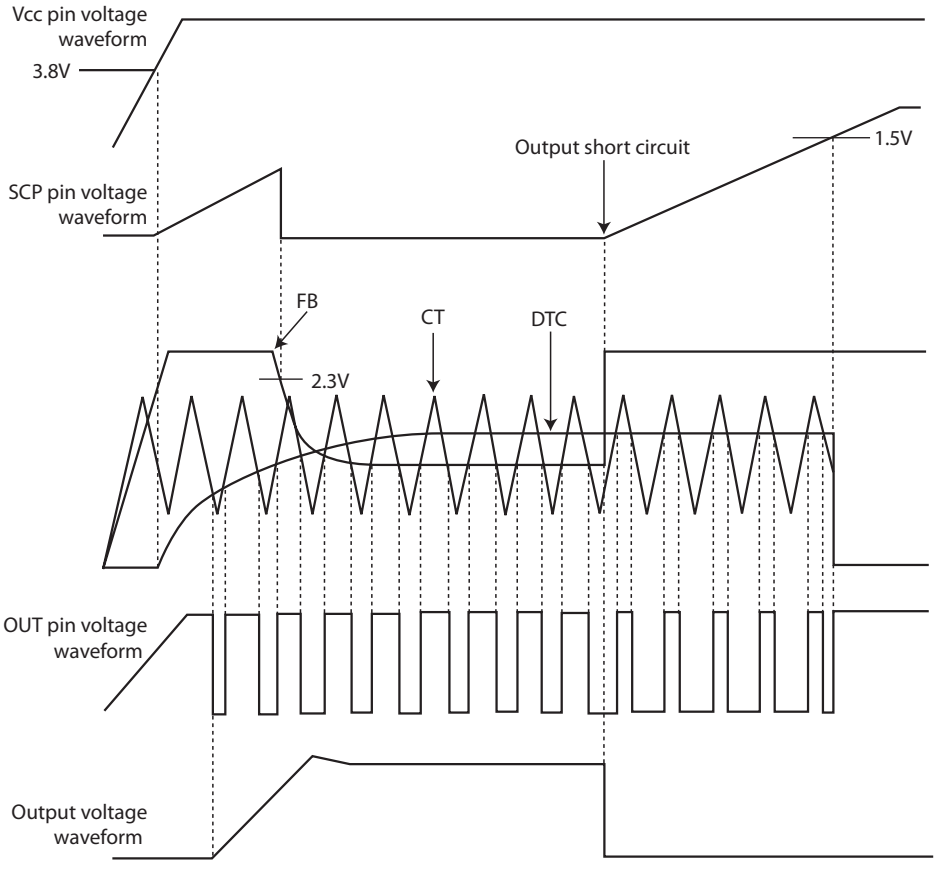
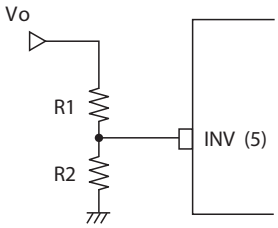


Fig.16 BD9851EFV Timing chart

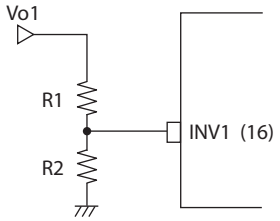
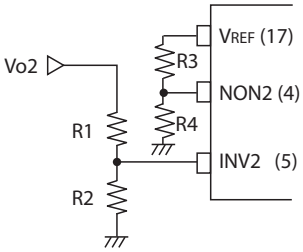
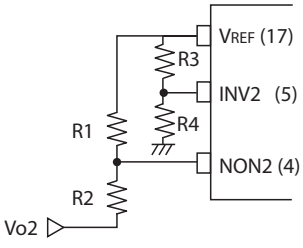
●Description of external components

• Setting of output voltage (BD9850FVM)

Setting of output voltage for the step-down application can be calculated by the formula below :

Setting procedure	Application
Vo = Vthea × (R1 + R2) / R2 [V] (Vthea: Error Amp threshold voltage Typ. 1.0 [V])	

●Setting of output voltage (BD9851EFV)

Setting procedure	Application
• Step-down (CH1), Step-up (CH1) Vo1 = Vthea × (R1 + R2) / R2 [V] (Vthea: Error Amp threshold voltage Typ. 1.0 [V])	
• Step-down (CH2) Vo2 = $V_{NON}2$ × (R1 + R2) / R2 [V] $V_{NON}2$ = 2.5 × R4 / (R3 + R4) [V] However, set the NON2 pin voltage to 0.3 to 2.0 V.	
• Inverting (CH2) Vo2 = 2.5 – {(2.5 - $V_{INV}2$) ¥ (R1 + R2) / R1} [V] $V_{INV}2$ = 2.5 × R4 / (R3 + R4) [V] However, set the INV2 pin voltage to 0.3 to 2.0 V	

●Setting of oscillation frequency (BD9850FVM)

Connecting a resistor to the RT pin (pin 2) allows for the setting of oscillation frequency.

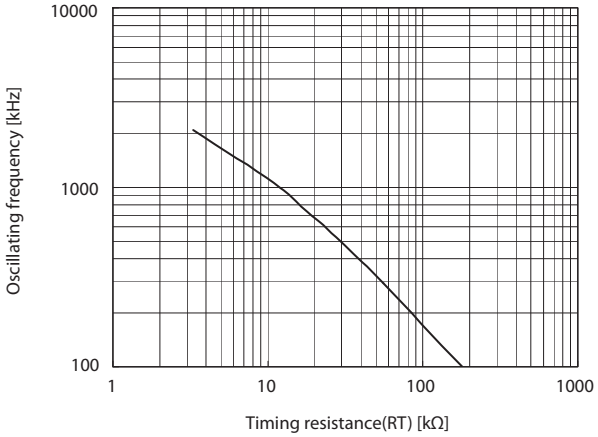


Fig.18 RT vs. Oscillation frequency

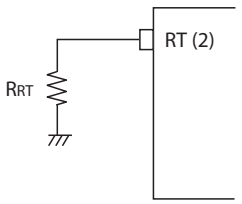


Fig.17 Setting procedure for BD9850FVM oscillation frequency

• Setting of oscillation frequency (BD9851EFV)

Connecting a resistor to the RT pin (pin 2) and a capacitor to the CT pin allows for the setting of oscillation frequency.

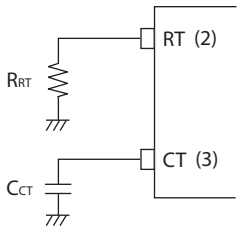


Fig. 19 Setting procedure for BD9851EFV oscillation frequency

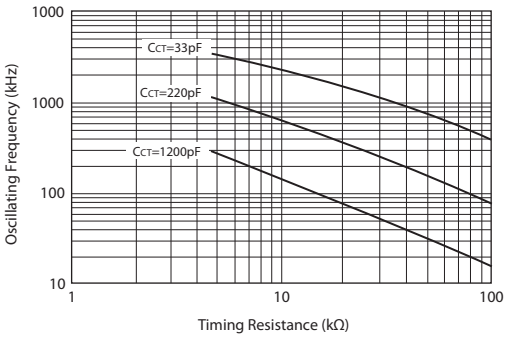


Fig. 20 RT vs. Oscillation frequency

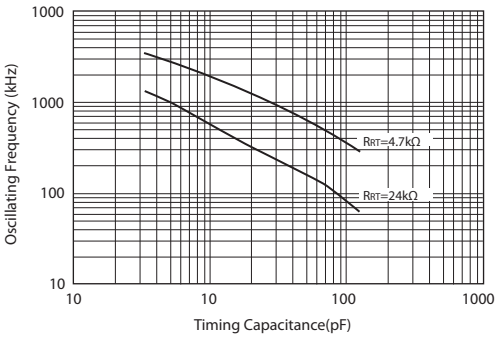
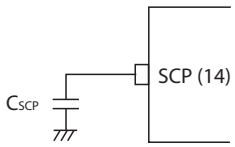


Fig. 20 CT vs. Oscillation frequency

• Setting of timer of short circuit protection circuit (BD9851EFV)

Setting procedure	Application
$T_{SCP} = 7.45 \times 10^5 \times C_{SCP}$ T_{SCP} : Time from output short circuit to latch stop [sec] O_{SCP} : Capacitance of capacitor between the SCP and GND pins [F]	

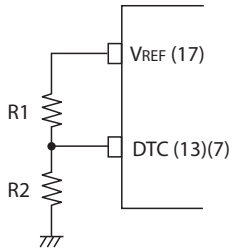
• Setting of maximum duty (BD9851EFV)

Setting procedure

$DUTY(max.) = 100 \times (V_{DTC} - Vth0) / (Vth100 - Vth0)$
$V_{DTC} = 2.5 \times R2 / (R1 + R2)$

DUTY(max.)	: Maximum duty [%]
V_{DTC}	: DTC pin voltage [V]
Vth0	: 0% duty threshold voltage [V]
Vth100	: 100% duty threshold voltage [V]

Application



• Pin treatment of unused channels (BD9851EFV)

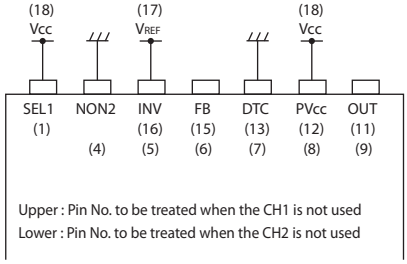
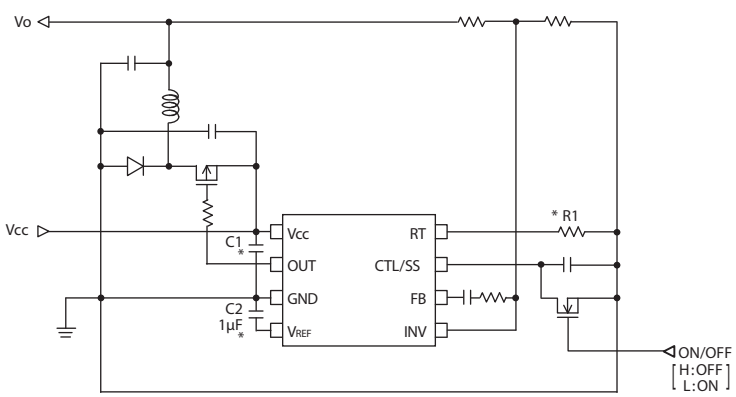


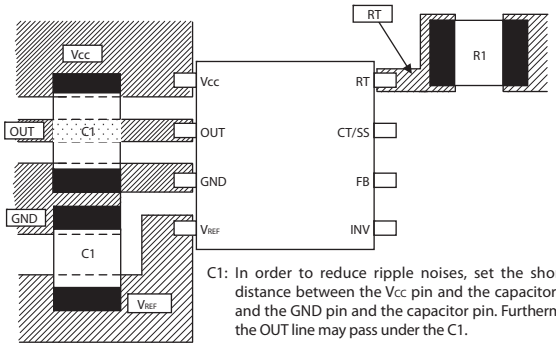
Fig. 22 Pin treatment procedure for unused channel on BD9851EFV

In order to use one channel, treat the pins of unused channel as shown above.

● Application circuit / Directions for pattern layout

(BD9850FVM)





C1: In order to reduce ripple noises, set the shortest distance between the V_{CC} pin and the capacitor pin, and the GND pin and the capacitor pin. Furthermore, the OUT line may pass under the C1.

C2: In order to reduce ripple noises, set the shortest pattern between the V_{REF} pin and the capacitor pin, and the GND pin and the capacitor pin.

R1: In order to stabilize the switching frequency, set the smallest pattern area so that PCB parasitic capacitance for the RT pin will be minimized.

Fig.23 BD9850FVM Reference application

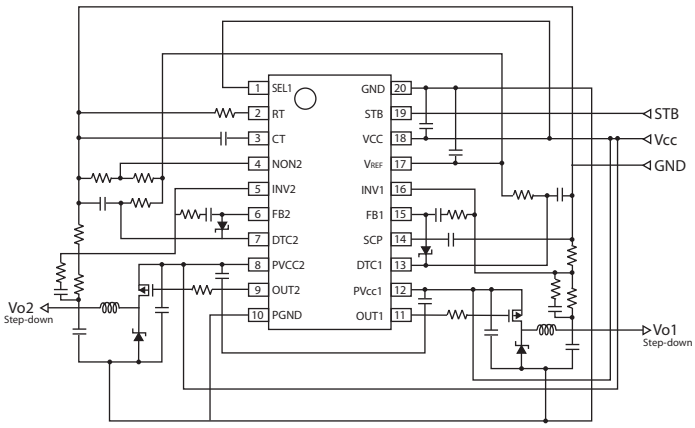


Fig.24 Step-down/Step-up application

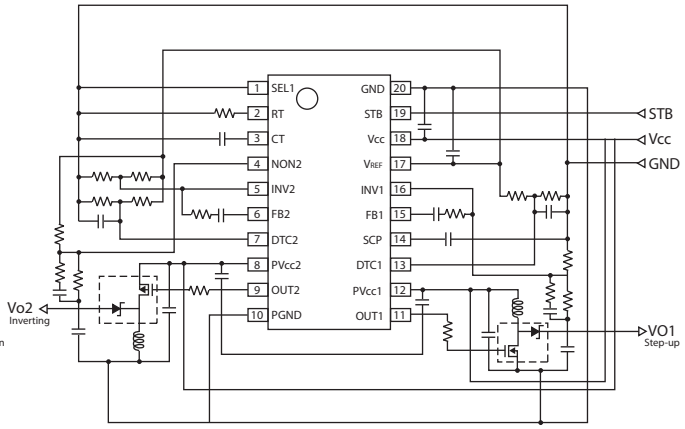


Fig.25 Step-up/Inverting application

● Equivalent circuit

(BD9850FVM)

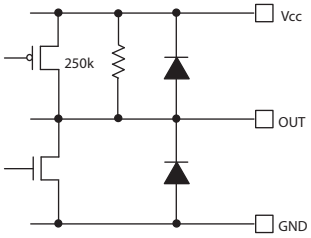
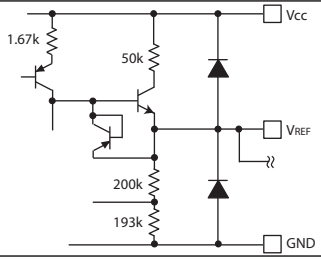
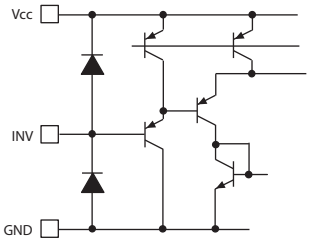
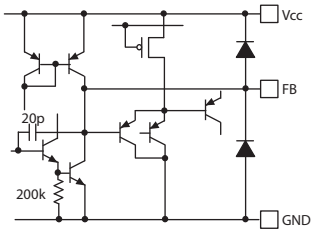
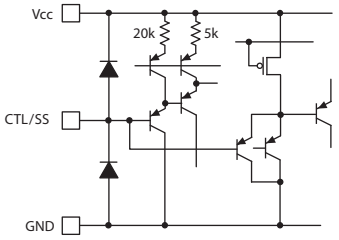
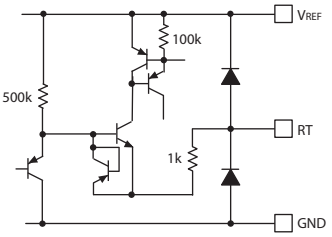
2PIN(OUT)	4PIN(V_{REF})	5PIN(INV)
		
6PIN(FB)	7PIN(CTL/SS)	8PIN(RT)
		

Fig.26 Equivalent circuit (BD9850FVM)

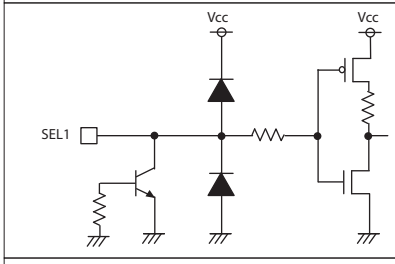
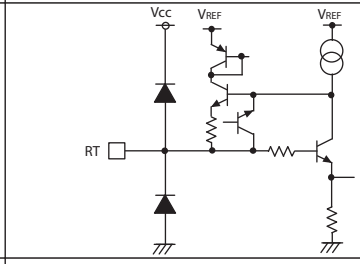
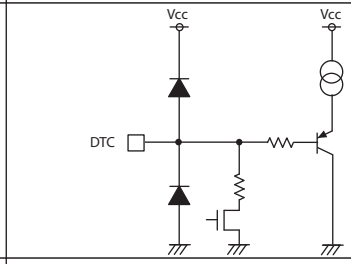
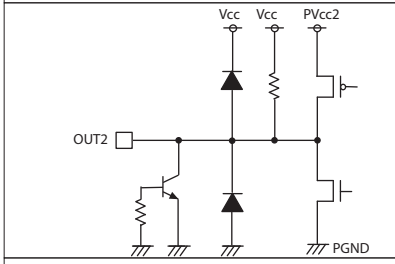
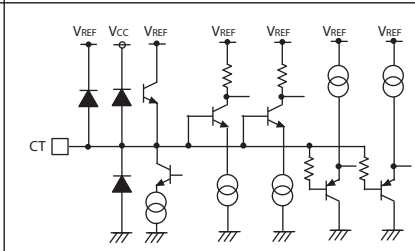
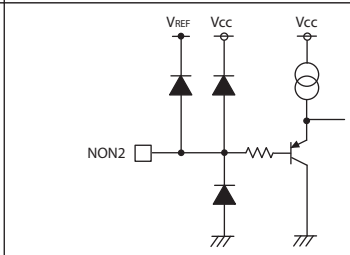
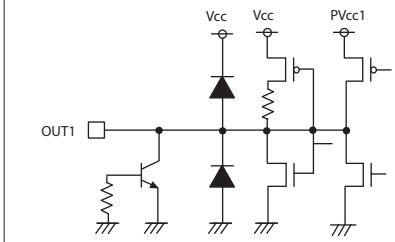
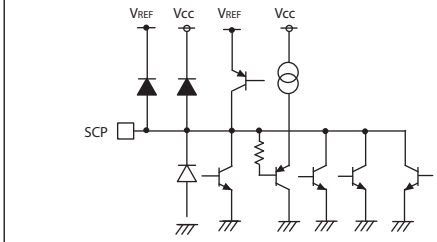
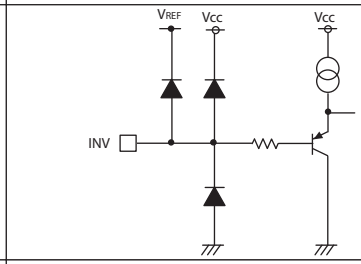
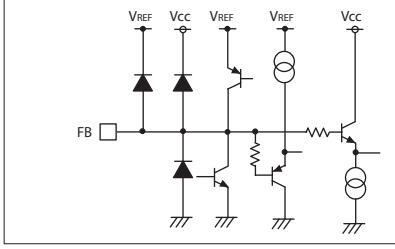
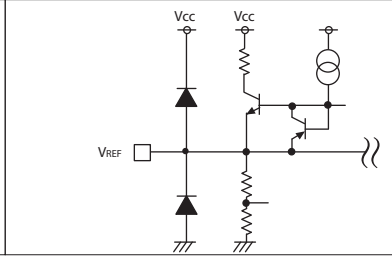
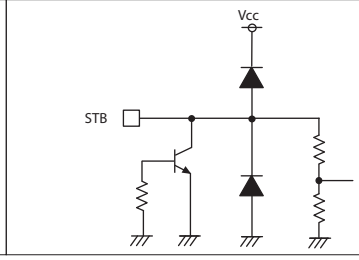
1PIN (SEL1)	2PIN (RT)	7,13PIN (DTC2,DTC1)
		
9PIN (OUT2)	**3PIN (CT)**	**4PIN (NON2)**
		
11PIN (OUT1)	**14PIN (SCP)**	**5,16PIN (INV2,INV1)**
		
6,15PIN (FB2,FB1)	**17PIN (V_{REF})**	**19PIN (STB)**
		

Fig.27 Equivalent circuit (BD9851EFV)

●Cautions on use

1) Absolute maximum ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2) GND potential
Ground-GND potential should maintain at the minimum ground voltage level. Furthermore, no terminals should be lower than the GND potential voltage including an electric transients.

3) Thermal design
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Inter-pin shorts and mounting errors
Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if positive and ground power supply terminals are reversed. The IC may also be damaged if pins are shorted together or are shorted to other circuitís power lines.

5) Operation in strong electromagnetic field
Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

6) Thermal shutdown circuit (TSD circuit)
The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

7) Testing on application boards
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to, or removing it from a jig or fixture, during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting and storing the IC.

8) IC pin input

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements to keep them isolated. Pin junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When GND > Pin A and GND > Pin B, the Pin junction operates as a parasitic diode.

When Pin B > GND > Pin A, the PñN junction operates as a parasitic transistor.

Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

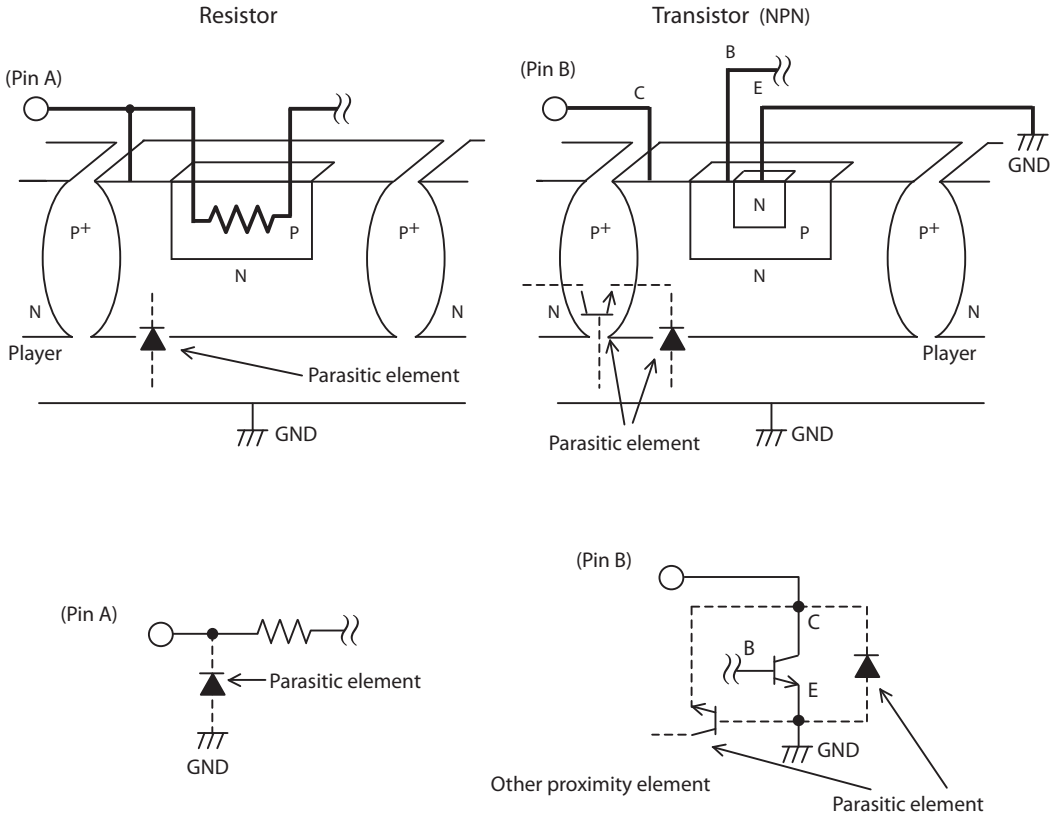


Fig. 28 Typical simple construction of monolithic IC

9) Common impedance

The power supply and ground lines must be as short and thick as possible to reduce line impedance. Fluctuating voltage on the power ground line may damage the device.

10) On the application shown below, Vcc is short-circuited to the Ground with external diode charged, internal circuits may be damaged. recommended to insert a backflow prevention diode in series with the Vcc or a bypass diode between each pin and Vcc.

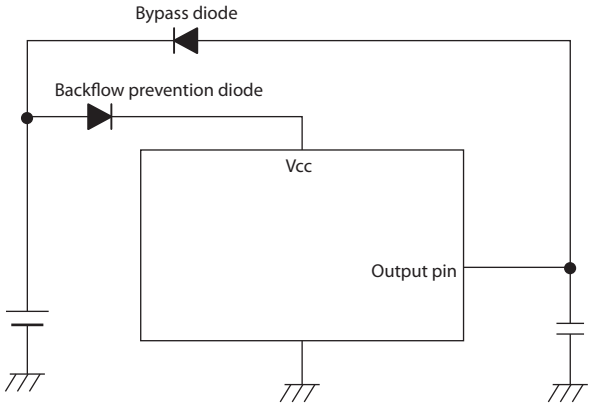


Fig. 29

11) Although ROHM is confident that the example application circuit reflects the best possible recommendations, be sure to verify circuit characteristics for your particular application. Modification of constants for other externally connected circuits may cause variations in both static and transient characteristics for external components as well as this Rohm IC. Allow for sufficient margins when determining circuit constants.

Oscillation frequency setting resistor

12) For the oscillation frequency setting resistor to be inserted between the RT pin and the GND pin, mount this resistor close to the RT pin and provide the shortest pattern routing.

●Thermal derating characteristics

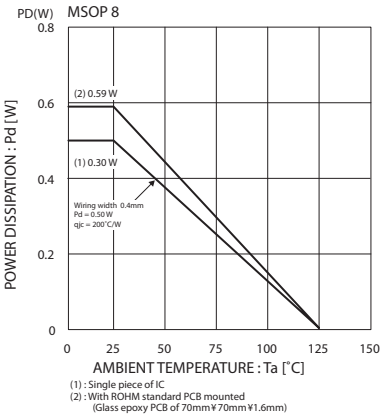


Fig.30

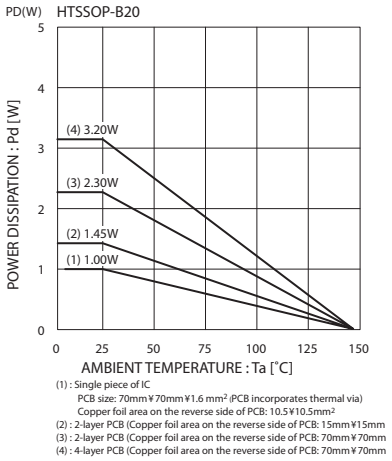


Fig.31

●Selection of order type

B	D	9	8	5	0	F	V	M	—	T	R

ROHM model name	Product No. 9850=10V 9851=20V	Package type FVM=MSOP8 EFV=HTSSOP-B20	Taping type TR=Reel-type embossed carrier tape (MSOP8) E2=Reel-type embossed carrier tape (HTSSOP-B20)

MSOP8

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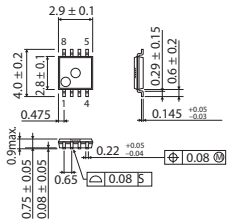
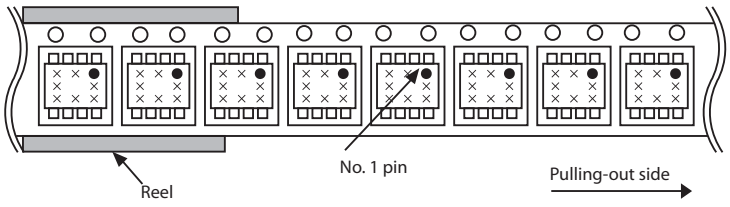


(unit : mm)

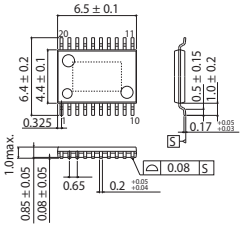
<Package specifications>

Package style	Embossed carrier tape
Quantity	3000 pieces/reel
Packaging direction	TR (When holding a reel in left hand and pulling out the tape with right hand, No. 1 pin appears in the upper right of the reel.)



HTSSOP-B20

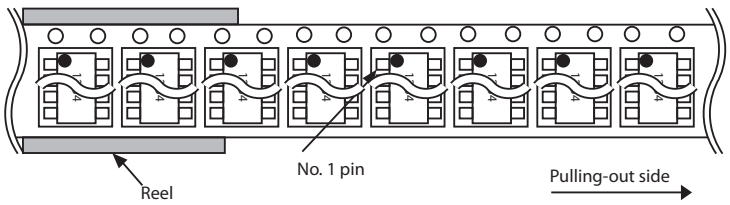
<Dimension>



(unit : mm)

<Package specifications>

Package style	Embossed carrier tape (Moisture-proof specificatin)
Quantity	2500 pieces/reel
Packaging direction	E2 (When holding a reel in left hand and pulling out the tape with right hand, No. 1 pin appears in the upper left of the reel.)



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